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Investigation of the Switching States in the Asymmetrical Hybrid Cascaded Multilevel Inverter

Alseddig Elzowawi
Misurata University
Assdig_z@yahoo.com

Mustafa Elsherif
Misurata University
m.a.m.elsherif@gmail.com

Abstract— **Cascaded multilevel inverter with unequal DC sources shows better performance in terms of the number of voltage steps at the output voltage than with equal DC sources, since the number of steps is higher when using unequal DC sources. Therefore, the output voltage waveform is improved and become closer to the sine wave. This in turn will reduce the harmonic content in the output waves. However, obtaining a separate DC source in every single cell in the inverter is difficult and costly, especially these sources are not equal (have different values) according to the used voltage ratio. Thus, hybrid cascaded multilevel inverter could offer a good solution, by using only one DC source and replacing the other sources with capacitors. However, a key challenging of this transformation is regulating the voltage of these capacitors at the specified values. This paper examines the significance of switching states redundancies of the voltage ratios on the capacitors balancing. Hence, a three-cell hybrid cascaded multilevel inverter with different voltage ratios has been modeled and simulated.**

Index Terms— **Hybrid Cascaded Multilevel Inverter, Unequal DC Sources, redundancy, Capacitors.**

I. INTRODUCTION

In power electronics topologies, the components number of the circuit and the quality of the output waves are significant factors that determine the best topology for the application. Multilevel inverters have numerous different topologies. However, cascaded H-bridge multilevel inverter has proved significant potentials if compared with other conventional multilevel inverters [1].

Cascaded multilevel inverter is the connection of two or more of H-bridge converters in series. Providing each H-bridge (HB) with a separate DC source. Depending on the values of these DC sources, this inverter can be classified into firstly, symmetrical inverter, which has equal DC values. Secondly, asymmetrical inverter, which has different DC values.[1– 3]. Asymmetrical Cascaded multilevel inverter is better than the symmetrical inverter in terms of the device number, voltage steps and the total harmonic distortion (THD), because this inverter can generate output voltage wave with higher number of steps[4]. Consider that, there are three cascaded multilevel inverters, the first is symmetrical with three H-bridges, hence, the maximum output voltage of this inverter is ($3V_{DC}$), and the number of staircase steps (m) is 7steps according to (1).

$$m=2N+1 \quad (1)$$

Where N is the number of connected H-bridges. This type of inverters could also categorized as order one inverter [2], [4].

However, the second inverter is asymmetrical inverter, i.e. isolated unequal DC source connected with each H-bridge. Thus, several variable output voltages can be obtained, depending on the voltage ratios between the DC sources of the three cell. For instance, if the ratio is $1V_{DC}$, $2V_{DC}$ and $4V_{DC}$, the maximum output voltage will be ($7V_{DC}$) with 15 voltage levels in the waveform [5]. Some of the levels were generated directly from the DC sources, and the others were generated by a combination of two or three DC sources (cells) with different signs, like ($5V_{DC}$) voltage step, this could be achieved by adding $1V_{DC}$ to $4V_{DC}$, or adding $-1V_{DC}$ to $2V_{DC}$ and $4V_{DC}$.

The voltage levels that necessary need a mixture of two or more DC sources are called derived levels; this also means more switching (SW) states (redundancies) for that voltage level [1]. The inverter that has a voltage ratio that follows a binary manner such this inverter is categorized as order two, and the number of levels can be obtained by (2)[1].

$$m=2^{N+1}-1 \quad (2)$$

This type of inverter in turn produces considerably enhanced output voltage than the symmetrical inverter, as it has higher maximum voltage and improved voltage wave with less total harmonic distortion THD. Thus, the asymmetrical inverter offers higher number of voltage steps in the output voltage than the symmetrical inverter with the same number of H-bridges.

Furthermore, if the voltage ratio among the sources is following the ternary mode (the power of three), then the inverter is classified as order 3. The simplest ratio of this mode with three cells is $1V_{DC}$, $3V_{DC}$ and $9V_{DC}$. Thus, the maximum voltage will be $13V_{DC}$ with 27 voltage steps, which follows (3)[1]:

$$m=3^N \quad (3)$$

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This type of mode provides the highest number of voltage steps in the output voltage. Therefore, the output waveforms in this mode will be significantly enhanced than the previous inverters.

In spite of that, several other voltage ratios, which do not follow any of the modes mention above, could also be employed to obtain more voltage steps in the output voltage as illustrated in table I [6 –7].

The number of voltage steps generated by the different ratios could be calculated by the equation (4) [1].

$$m=2(V_{C1}+V_{C2}+V_{DC}) +1 \quad (4)$$

The voltage ratios shown in table I are extremely difficult to provide in reality as DC voltage sources, since this will lead to a greater cost and complexity to the inverter, as extra components would be used to attain the exact voltage required for the DC source for each H-bridge. Based on that, reforming this inverter would give better solution. This is done by keeping only one DC source in one H-bridge and changing the other sources with capacitors in the rest of the cells. This inverter is named Hybrid cascaded multilevel inverter (HCMLI).

However, the control scheme of the inverter should be able to let these capacitors have specific voltage levels according to the employed voltage ratio. This is a significant advantage, since the voltage ratio might be easily changed, as the capacitors can be charged to different voltage levels, when the voltage ratio of the inverter wanted to be changed, without much change in the circuits of the inverter and its control[8].

On the other hand, the voltage of these capacitors need to be continuously regulated at the desired voltages, therefore the output voltage can be synthesized correctly. Furthermore, extra attention should be paid to the regulation process, because the capacitors have different voltage values based on the voltage ratio between them. Consequently, in order to have a good regulation for each capacitor, the capacitor should be charged when it needs to be charged and discharged when it requests to be discharged.

In view of all that, the switching states for every voltage step must be carefully selected depending on the sign of the current, with the purpose of the capacitor to maintain the voltage level without charging or discharge over the limit.[9]

TABLE I. THE INPUT VOLTAGE RATIOS AND THE OUTPUT VOLTAGE LEVELS

No	Voltage Ratios			No. of levels	No. of redundancy levels	No. of redundancies /No of levels
	HB1 (V_{C1})	HB2 (V_{C2})	HB3 (V_{DC})			
1	1	1	1	7	5	71.42%
2	1	1	2	9	7	77.77%
3	1	1	3	11	9	81.81%
4	1	1	4	13	11	84.61%
5	1	1	5	15	9	60%
6	1	2	2	11	7	77.77%
7	1	2	3	13	9	81.81%
8	1	2	4	15	8	53.33%
9	1	2	5	17	10	58.82%
10	1	2	6	19	8	42.1%
11	1	2	7	21	6	28.57%
12	1	3	3	15	9	60%
13	1	3	4	17	9	52.94%
14	1	3	5	19	8	42.10%
15	1	3	6	21	6	28.57%
16	1	3	7	23	4	17.39%
17	1	3	8	25	2	8%
18	1	3	9	27	0	0%

Thus, this research offers some important insights into the impact of the switching states redundancies on the regulation process of the capacitors voltages, and hence its effect on the operation of the inverter in general.

II. SWITCHING STASTES NUMBER

The number of redundancy levels in table I indicates the number of voltage levels that has more than one switching state (i.e more than one method to achieve the voltage level by using the three cells). For instance, the voltage ratio No. 1, which is (1, 1, 1), has five voltage steps that have more than one switching state (2, 1, 0, -1, -2), as can be seen in table II. Step 2 for example has three methods to achieve it, (1, 1, 0) or (1, 0, 1) or (0, 1, 1).

TABLE II. THE VOLTAGE RATION (1, 1, 1) AND THE NUMBER OF SWITCHING STATES

Steps	Voltage step	No. of Switching states
3	300	1
2	200	3
1	100	6
0	0	7
-1	-100	6
-2	-200	3
-3	-300	1

From table I, it is apparent that, the number of redundancy levels is either an odd or even number. The odd number means that the zero voltage step is counted, since there are several methods to produce it, whereas the even number indicates that the zero step is not counted as it has only one way to generate it.

In addition, the voltage ratios illustrated in table I may possibly be classified into three groups, the first group can be named as low voltage ratios, which is from No. 1 to 5. This group of ratios produces the lowest voltage steps numbers compared with the other categories. Since the highest number of steps is 15. The second group might be called medium voltage ratios, from No. 6 to 11. The upper number of voltage levels that could be generated by this category is 21. The third class is high voltage ratios, from No. 12 to 18, with top of 27 voltage levels.

However, when looking at the switching states number in each group, it is obvious, that group one has the greatest number of redundancy levels with 11 levels. This means that there are 11 levels have more than one switching states. While, the medium voltage ratios have 10 redundancy levels as the top, and the maximum redundancy levels in the third group is 9.

III. CIRCUIT CONFIGURATIONS

The HCML inverter considered in this paper consists of three H-bridges, the first cell contains separate DC source, and the other two cells have separate capacitors. All the three cells connected in series. Then the inverter was connected with R-L load as depicted in Fig 1. Generally, in this paper the DC source takes the highest value of the voltage ratio as shown in table I. This may be due to four reasons. Firstly, to provide enough energy to charge the two capacitors. Secondly, to quickly charge the capacitors as they set to lower voltage levels. Thirdly,

to have a regular value rather than a percentage of the highest value. Fourthly, it becomes easier to change the voltage ratio with the same DC source when needed, as in case B and C in the next section. Table III shows the parameters of the inverter.

TABLE III. THE VALUES OF THE INVERTER'S PARAMETERS

Parameters	Values
R	0.5Ω
L	0.015H
C_1	2.4mF
C_2	2.4mF

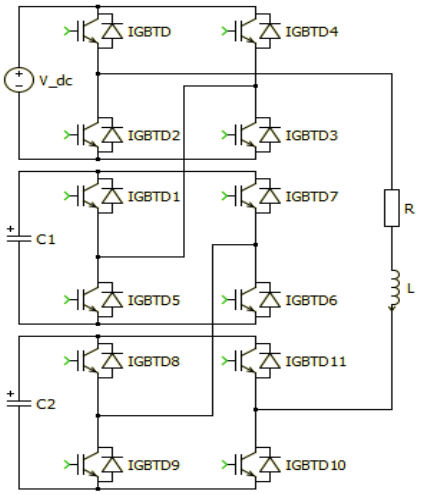

Figure 1. The configuration of the circuit.

Furthermore, phase shift pulse width modulation (PSPWM) was chosen to control the inverter, as it is one of the most popular modulation schemes. There will be one sine wave (reference wave) with frequency of 50Hz, and a number of carrier waves are according to (5).[10]

No. of carriers= (total number of steps -1)/2 (5)

The frequency of the carriers is 250Hz, and there is a certain phase shift among the carriers will be applied to create the phase shift among the output voltage of the three H-bridges. Then, these carriers are compared with the reference wave, and the modulation index was set to the value (0.93) in order to obtain the correct levels.

The inverter was modeled and simulated using Plecs software, and the controller of the inverter is a program coded by C language. This controller performs the comparison between the sine wave and the carriers, and it receives feedbacks from the load current and voltage of the two capacitors. Based on that, the controller chooses the state of each cell (1or 0 or -1) and provides the switching states for the switches in all cell. The output voltage of the inverter is the sum of the output voltages of the three cells, thus, the correct voltage steps are synthesized and the voltage of the two capacitors are maintained at the desired level.

IV. SIMULATION OF THE CONSIDERED INVERTERS

In order to understand the influence of the switching states redundancy of the voltage ratios on the operation of the inverter, and on the capacitors voltage regulation, a number of voltage ratios will be examined and analyzed. This is accomplished by employing these ratios in the simulated inverters to generate 7, 15, 17, 19, 21 and 27 steps staircase waves.

A. Voltage ratio (1, 1, 1)

This voltage ratio is from group one (low voltage ratios), which produces symmetrical hybrid cascaded multilevel inverter, as the voltage source and the two capacitors will have the same voltage values. The total number of steps is seven, and there are five voltage steps have switching states redundancies as shown in table II. The DC voltage source value is 100V, and the two capacitors are regulated at 100V too. Therefore, the maximum output voltage will be 300V. The output voltage and voltages of the capacitors are depicted in Figs (1) and (2) respectively.

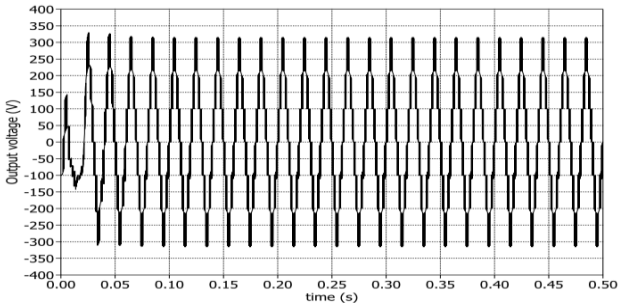

Figure 2. Output voltage when (1, 1, 1) ratio was applied.

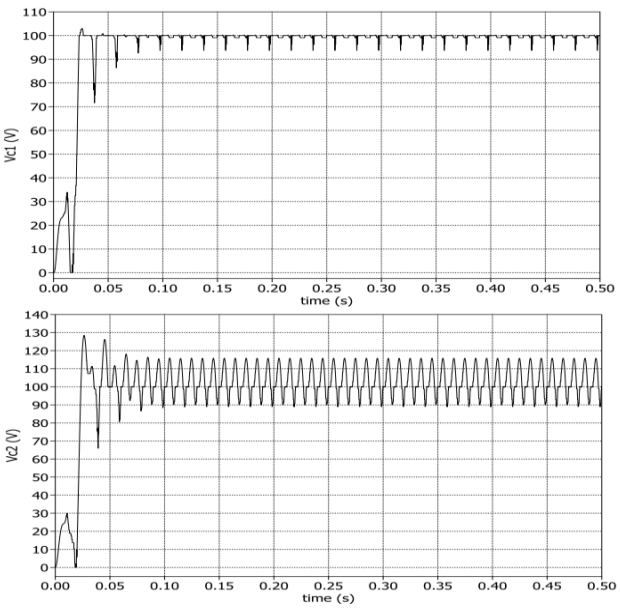

Figure 3. Capacitors voltages when (1, 1, 1) ratio was applied.

As can be seen from the output voltage figure that the voltage was synthesized correctly, and the wave has a good staircase shape. Besides, the voltages of the capacitors were maintained properly at the specified values as clearly shown in Fig (3). The voltage of capacitor 1 shows better regulation than the voltage of capacitor 2, which is due to the selection of the switching states was in favor of the capacitor 1 over capacitor 2.

Consequently, the operation of the inverter considered successful, and it was easy to maintain the voltage of the capacitors, as the redundancy percentage of the switching states is very high, since most of the voltage steps have several switching states (5 steps out of 7, i.e it is 71.4% from all steps). This aids with the decision making to select the best switching state suitable to regulate the

voltage of the capacitors. However, the number of steps generated by this ratio is low (seven steps).

B. Voltage ratio (1, 2, 4)

The considered voltage ratio follows order two (binary manner) and it is from group two (medium voltage ratios), it produces asymmetrical hybrid cascaded multilevel inverter with 15 voltage steps. Only 8 steps out of 15 (53.33%) have redundancies, as shown in table I. The voltage of the second capacitor is balanced at 50V, the first capacitor at 100V, and the DC source is 200V. Hence, the maximum generated output voltage will be 350V. Figs (4) and (5) illustrate the results of the inverter operation.

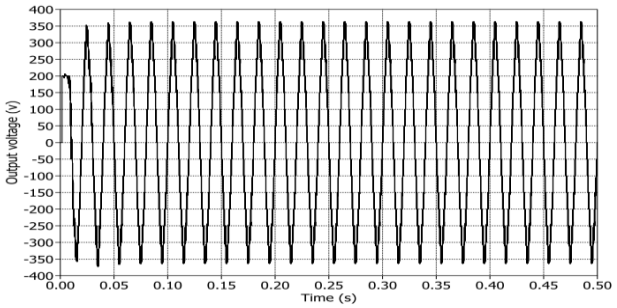

Figure 4. Output voltage of (1, 2, 4) ratio.

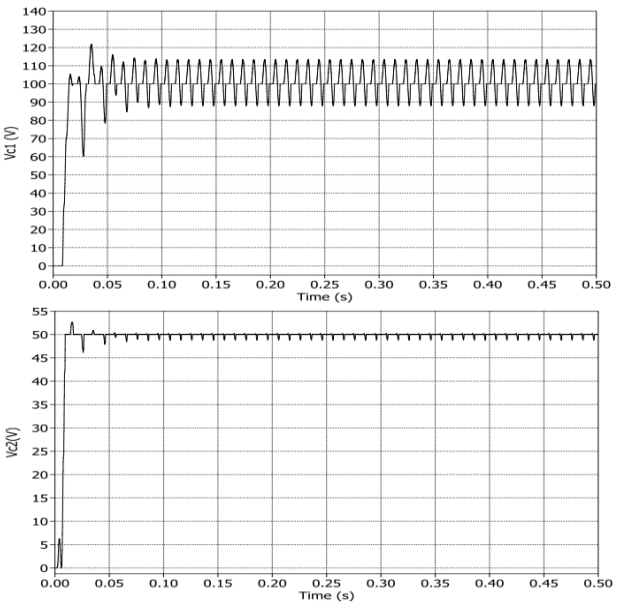

Figure 5. Capacitors voltages of (1, 2, 4) ratio.

Fig (4) shows that the output voltage waveform was properly produced with 15 voltage levels. In addition, the voltages of the two capacitors were accurately regulated as can be seen from Fig (5). In contrast, of case B, the voltage of capacitor 2 demonstrations better regulation than capacitor 1, as the selection of the switching states was in favor of the capacitor 2 over capacitor 1.

Therefore, the regulation process performed by the controller was effective; despite of the percentage of the redundancy was (53.33%). This means that about half of the switching states of this ratio have redundancies, and the controller still can make the inverter successfully maintains the voltages of the capacitors without changing anything in the inverter's circuit.

C. Voltage ratio (1, 3, 4)

This voltage ratio is taken from group number three (high voltage ratios), which delivers 17 voltage steps by the asymmetrical hybrid inverter. Nine voltage levels (52.94%) have redundancies, as revealed in table I. The voltage of the second capacitor is set at 50V, while the first capacitor at 150V and the DC source is 200V. Thus, with these values the top voltage will be generated is 400V. Figs (6) and (7) depict the output voltage waveform and the voltages of the two capacitors respectively.

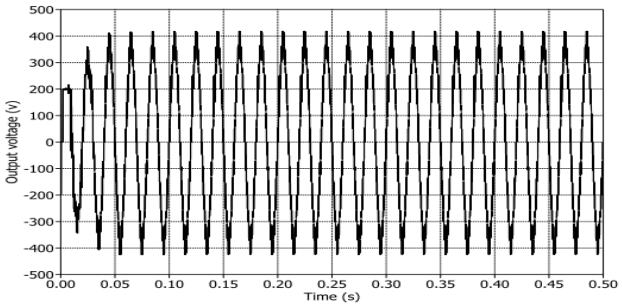

Figure 6. Output voltage of (1, 3, 4) ratio.

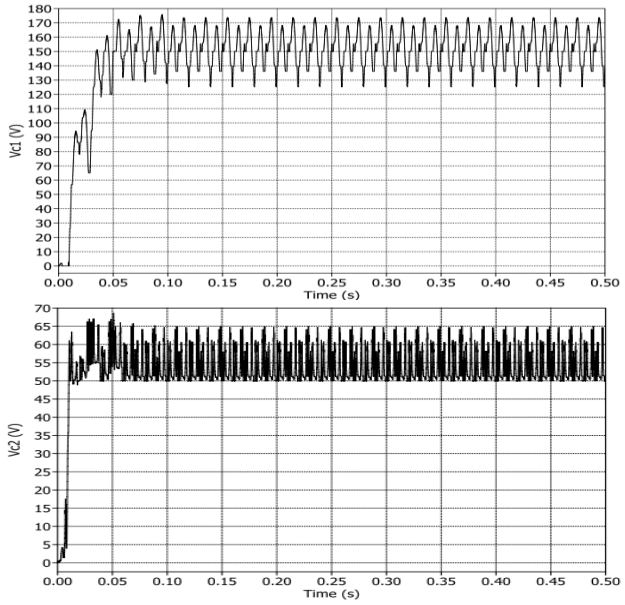

Figure 7. Capacitors voltages of (1, 3, 4) ratio.

By observing the figures above, it is clear that the voltages of the capacitors were maintained at the specified values, this in turn let the inverter manage to build the output voltage correctly. On the other hand, the variations of both capacitors voltages are larger than those in case A and B. This seems due to the limited switching states redundancies, since the parameters values of the inverter have been kept constant as the previous cases. Furthermore, it is possible to decrease these variations by changing some of the parameters in the inverter, but this would make the performance of the inverter limited to a certain load values.

D. Voltage ratio (1, 3, 5)

In this section, another voltage ratio was selected from the high voltage ratios, which also composites asymmetrical inverter and synthesizes 19 output voltage levels, with only (42.10%) from all levels have redundancies. Therefore, this redundancy percentage will

be examined to see if the inverter can regulate the capacitors. In order to apply this ratio, certain voltages have been employed, the voltage of C_2 is 50V, whereas the voltage of C_1 is 150V, and the DC source value is 250V. Thus, the peak load voltage is 450V. When the voltage ratio was applied to the inverter, the controller could not regulate the capacitors voltages, and the output voltage was not constructed correctly, until the inductance of the load was changed to (0.05H). Then, the inverter was properly working as shown in Figs (8) and (9).

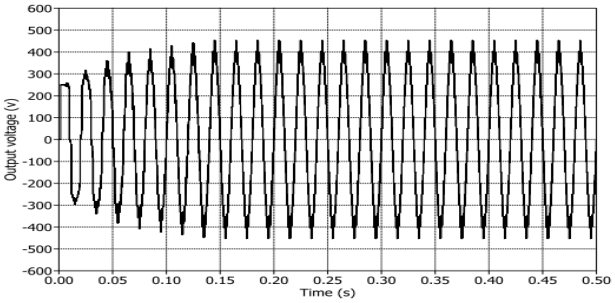

Figure 8. Output voltage of (1, 3, 5) ratio.

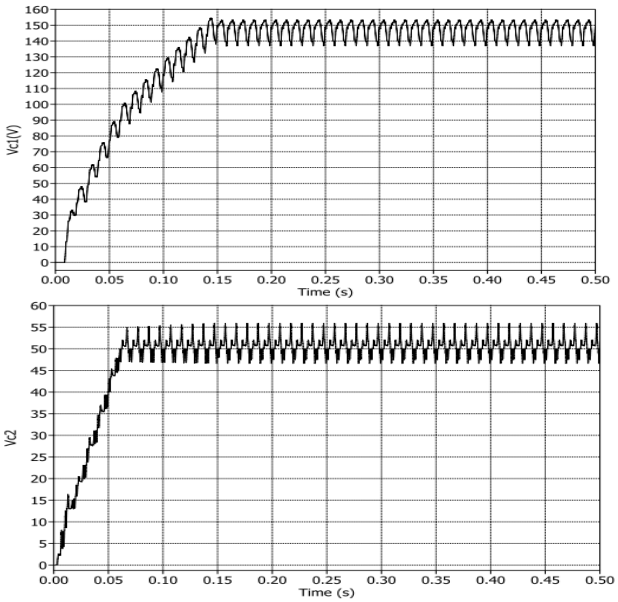

Figure 9. Capacitors voltages of (1, 3, 5) ratio.

Changing the load inductance has two advantages, the first one, it made the load current lag the voltage with larger angle (low power factor), so that the selected switching states have become more effective in balancing the capacitors [11]. The second benefit is that it has reduced the load current, thus, the discharge current of both capacitors was minimized. Therefore, the controller managed to regulate the capacitors voltages, and generate good output voltage waveform as depicted in Fig (8). However, the greater inductance caused longer charging time for both capacitors as can be seen from Fig (9), which is due to the reduced current value flowing in the inverter. As a result, the reduced number of redundancies (42.10%) let the regulation process of the capacitors and the operation of the inverter to be more challenging. The new inductance will also be used in next cases.

E. Voltage ratio (1, 3, 6)

The present ratio is also from the third group. The number of voltage levels generated by this ratio is 21 levels, but there are only six steps out of 21 have redundancies (28.57%). In this inverter, the considered voltage for each cell is 50V for C_2, 150V for C_1, and 300V for the DC source. Therefore, the maximum voltage of the output voltage should be 500V.

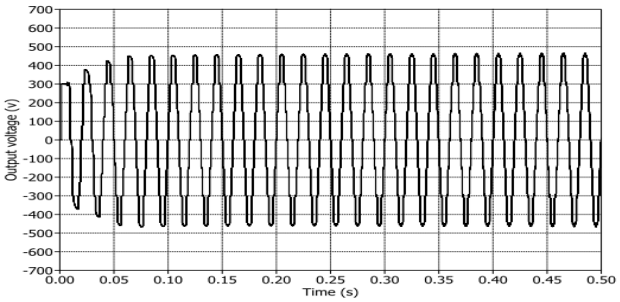

Figure 10. Output voltage of (1, 3, 6) ratio.

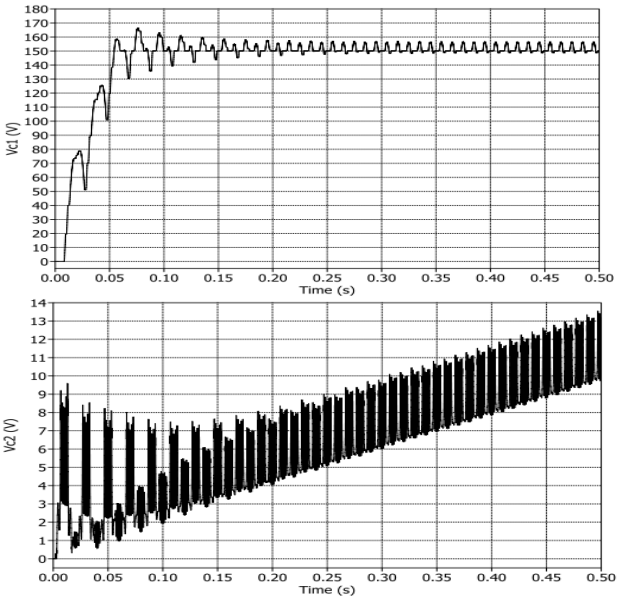

Figure 11. Capacitors voltages of (1, 3, 6) ratio.

Based on the results from Fig 10 and Fig 11, it can be said that the inverter did not operate properly, and could not maintain the voltages of the capacitors. In spite of the changes that have been applied to the inverter, but the controller was not able to maintain the voltages of the capacitors. This was attributed to the low redundancies of the switching states (28.57%), so that the controller had very limited choices i.e it had to select the available switching state which is not suitable to the state of the capacitors (charging or discharging).

Although the controller managed to regulate one capacitor, but this did not let the inverter succeed in synthesizing the right output voltage, as capacitor one was in favor over the other capacitor when selecting the switching states.

In order to over come this problem, the second capacitor was replaced with a DC source, Figs 12 and 13 show that the inverter was operating perfectly, and the only capacitor in the inverter was accurately regulated at the precise voltage. This solution may not be the perfect solution, but it could be an alternative way instead of changing the parameters of the inverter and changing the controlling scheme.

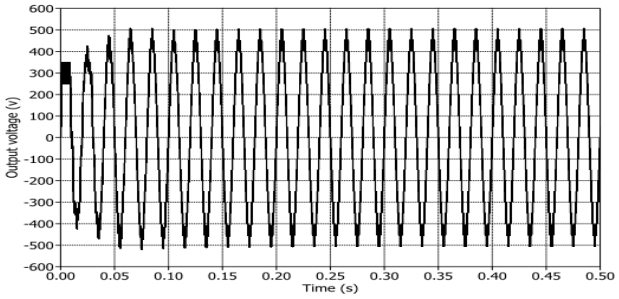

Figure 12. Output voltage of (1, 3, 6) ratio with 2 DC sources.

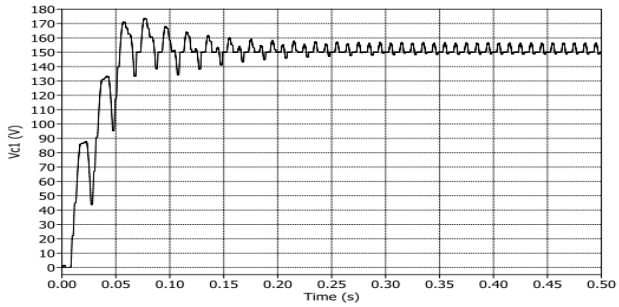

Figure 13. Capacitor voltage of (1, 3, 6) ratio with 2 DC sources.

F. Voltage ratio (1, 3, 9)

The last considered voltage ratio is (1, 3, 9), which follows the ternary mode, so that 27 levels should be synthesized by this ratio. However, there is no redundancies in this ratio at all, the employed voltages in this inverter are 50V for C_2, 150V for C_1, and 450V for the DC source, thus, the maximum output voltage should be 650V. The results obtained from the simulation are presented in Fig 14 and Fig 15.

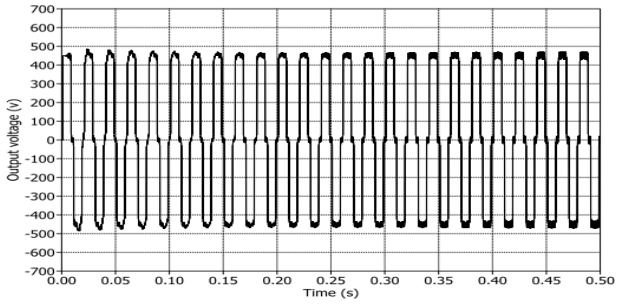

Figure 14. Output voltage of (1, 3, 9) ratio.

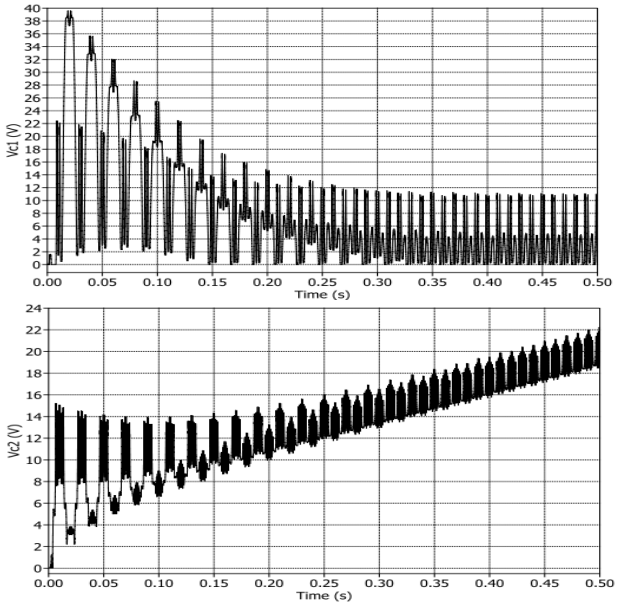

Figure 15. Capacitors voltages of (1, 3, 9) ratio.

From the results shown above, it can be seen that both capacitors have not been regulated at the desired voltages, which let the inverter did not perform properly. This is due to the controller could not drive the inverter in the right way, since there are no redundancies at all in the used voltage ratio, hence, it was impossible to maintain the voltages of the capacitors. When one of the capacitors was exchanged with a DC source, the controller could not also regulate the other capacitor. However, when both capacitors were replaced with DC sources, the output voltage was synthesized correctly as illustrated in Fig 16.

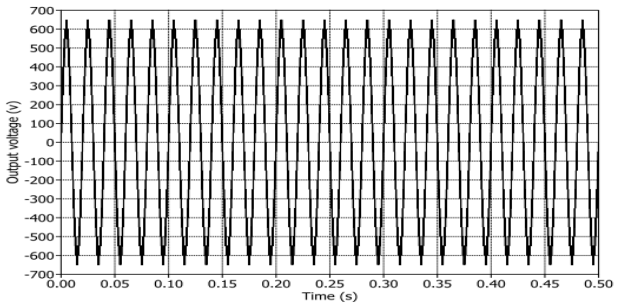

Figure 16. Output voltage of (1, 3, 9) ratio with 3 DC sources.

V. DISCUSSION

A number of voltage ratios have been utilized to operate a three cells hybrid cascaded multilevel inverter. From these cases, it can be said that as the redundancy levels decreases, it becomes harder for the control system to drive the inverter. So that some changes had to be performed to help the controller in driving the inverter, like in case D. These changes have affected the performance of the inverter and the charging time of the two capacitors, since both capacitors took longer time to charge to the specified levels. Moreover, under 42.10% redundancy ratio (more than 19 levels), the controller faced difficulties in regulating the capacitors. As the redundancy ratio became lower, it converted to impossible to drive the inverter and maintain the capacitors voltages with the considered control strategy.

In order to balance the capacitors, the voltage ratio has to provide adequate switching states for each voltage step, so that the controller can select the right switching state for the specific voltage level according to the state of the capacitors, and the sign of the current. Thus, it must be an available switching state suitable for charging the capacitors when they need to be charged, and another switching state for discharging the capacitors when they have to be discharged.

Furthermore, other switching states should also be available to charge one capacitor and discharge the other. All these scenarios should have suitable switching states to regulate the capacitors optimally. However, this is not the reality when using the voltage ratios shown in table I, since each voltage ratio has restricted redundancies. This has also affected the voltage variation of the capacitors, since there are limited redundancies, one capacitor has to be in favor over the other, thus, its voltage will be better than the other.

Based on the results, the best voltage ratios that have sufficient redundancies to properly drive the inverter and balance the capacitors are revealed in table IV.

TABLE IV. THE BEST VOLTAGE RATIOS

No of levels	Best voltage ratios	Voltage ratio group
7	(1, 1, 1)	Low group
9	(1, 1, 2)	Low group
11	(1, 1, 3)	Low group
13	(1, 1, 4)	Low group
15	(1, 1, 5), (1, 3, 3)	Low and high group
17	(1, 2, 5)	Medium group
19	(1, 2, 6), (1, 3, 5)	Medium and high group

From table IV, it can be seen that most of the best voltage ratios are from the low voltage group. Since this group offers highest number of redundancies, then the medium group and the last is the high voltage group.

VI. CONCLUSUON

Several simulation studies have been performed to investigate the influence of the switching redundancies on the regulation process of the capacitors. From these studies, it can be said that the redundancy ratio is very significant factor in balancing the capacitors and synthesizing the precise staircase output voltage. As the redundancy number increases, the easier the capacitors regulation process. This research has found that voltage ratios that have about 50% redundancies or more are able to balance the capacitors. However, the other ratios with less than 42.1% redundancies are very difficult in balancing the capacitors. As a result, when comparing the voltage ratios mentioned in table I, the best ratios are those shown in table IV. These ratios can be applied in the inverter and significantly help with the capacitors voltages regulation.

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