The International Journal of Engineering and Information Technology

journal homepage:www.ijeit.misuratau.edu.ly

Using Memristor Element to Improve the Reliability of Digital Circuits

Mohamed A. Abufalgha
Misurata University
m.a.abufalgha@eng.misuratau.edu.ly

Abstract— **Memristor has been used as a filter stage to improve The reliability of digital circuits has been improved by using memristor. This element works as a filter stage to waive most of the glitches generated in prior stages. The proposed technique is applied to three different circuits to improve their reliability. Those circuits are: a chain of inverters represents a long path topology, c432 benchmark represents a short path circuit, c1908 benchmark represents a long path circuit. The memristor stage is connected between the last two stages of each output path of the circuit. The memristance of the memristor is changed using a certain parameter (x_0), higher memristance means longer propagation delay and more glitches are attenuated. The experiment is run at different values of the memristance and the error probability is calculated at each value. The effect of this stage is studied by calculating the energy consumption and performance of the circuits with and without this stage. The Reliability-Energy-Performance trade-off relationship is found and introduced for each circuit, the results show that the reliability of the circuit is improved to the highest levels, when x_0= 9E-4, the glitches that occurred on the last stage only has been registered at the output, whereas all the glitches that generated in the prior stages are attenuated completely.**

Index Term: **digital circuits reliability, soft errors, single event transient (SET), reliability-energy-performance trade-off.**

I. INTRODUCTION

Soft errors are a temporary effect that can cause a faulty operation of integrated circuits for a period of time. The output of this faulty operation may be latched up by a flip flop or a register causing faulty results. One of the dominant causes of soft errors is neutron particles generated by the interaction of cosmic rays with the nuclei of atmospheric gases. Soft errors increased last decades because of the technology scaling that occurred in the integrated circuits industry. Technology scaling that including smaller sizes of transistors, higher operating frequencies, lower voltage levels, and a higher number of transistors on the same size of the chip. On the other hand, this scaling increases the susceptibility of digital circuits, so they become more sensitive to the effect of soft errors caused by neutron particles. The rate of neutron particles that hit devices at the terrestrial environment is fixed, but the voltage level that represents a certain logic level is decreased, and the charge that is needed to represent that logic level is reduced too [22]. Due to this, the charge that is needed to be collected from an interaction between a neutron particle and a sensitive node on a digital circuit to flip the state of that node become smaller. So despite the fact that the rate of the neutron particles is fixed, the range of effective particles increased due to the technology scaling. This effect can be noticed if we know that the Linear Energy Transfer (LET) that needed to cause a Single Event Transient (SET) in 1990 was 15MeV.cm^2/mg, where the LET values that is needed to cause a SET in 2004 is 2MeV.cm^2/mg [1]–[3].

The contribution of these soft errors on decreasing combinational circuits' reliability is a major concern, so many techniques are suggested to mitigate these effects on different levels. on system levels redundancy techniques are suggested, those techniques include hardware redundancy such as Triple Modular Redundancy (TMR), information redundancy such as Error Detecting and Correcting Codes (EDCC), and time redundancy, the drawbacks of these techniques are high area overhead, power consuming, and the performance is reduced dramatically. On circuit level; gate sizing techniques are suggested. On device level; Insulating substrates, and Wide band-gap substrates techniques are used [4], [5], [23].

In this paper, we propose a new technique to improve the reliability of digital circuits using a memristor element as a delay element. This element is used to eliminate the narrow glitches caused by low-energy particles, and for the wider glitches makes them narrower so the probability of these glitches being latched is decreasing.

The rest of the paper is organised as follow. Section II gives details on the memristor element, section III presents the proposed technique to use the memristor element as a filter to improve digital circuits reliability, section IV presents the simulation results, section V presents the effect of the memristor on a circuit parameters, and section VI concludes the paper.

Received 22 Dec , 2021; revised 29 Dec, 2021; accepted 7 Jan, 2022.

Available online 15 Jan, 2022.

II. MEMRISTOR DEVICE

A. Background

Memristor element is introduced by LEON O. CHUA in 1971 [6]. It is characterised by the relation between the charge q(t) and the flux-linkage $\varphi(t)$. The memristance M of a memristor can be defined by the relation $M = d\varphi_m/dq$, where M has a unit of memristance. The memristance of a memristor depends on the magnitude and the polarity of the applied voltage and the length of time that voltage has been applied. It is called memristor as a contraction for memory resistor because it behaves like a nonlinear resistor with memory. The memristor remains just a theory, until Stan William and his team from HP Laps implement a first model, they implement model as a 40-nanometre cube of titanium dioxide (TiO_2), it is constructed by two layers: The lower layer has a perfect 2 to 1 oxygen to titanium ratio, what makes it an insulator or semiconductor. The upper layer is missing 5% of its oxygen (TiO_{2-x}), these vacancies on the oxygen concentration make this layer conductive [7], [8].

B. Memristor model

The relationship between current and voltage can be characterised by three different main equations, each equation reflects the relationship between certain parameters on a specific stage. Formula (1) expresses the observed nonlinear hyperbolic sinusoidal relation in the metal-insulator-metal of the memristor operation, the hyperbolic behaviour causes an increase in the conductivity of the device if the applied voltage increases a certain threshold voltage. The I-V relation also depends on the state variable x(t), which controls the memristance of the memristor device.

$$I(t) = \begin{Bmatrix} a_1 x(t)\sinh(\mathrm{bV}(t)), \mathrm{V}(t) \geq 0 \\ a_2 x(t)\sinh(\mathrm{bV}(t)), \mathrm{V}(t) < 0 \end{Bmatrix} \quad (1)$$

The threshold voltage that must be exceeded is implemented by the function $g(V(t))$in (2).

$$g(V(t)) = \begin{Bmatrix} A_p\left(e^{V(t)} - e^{v_p}\right), V(t) > \mathrm{v}_p \\ -A_n\left(e^{V(t)} - e^{v_n}\right), \mathrm{V}(t) > -v_n \\ 0, -V_n \leq V(t) < \mathrm{V}_p \end{Bmatrix} \quad (2)$$

where V_p and V_n, represent the positive and negative threshold, and theyare the magnitude exponential. The relations that model the state variable $f(x(t))$can be seen in (3),(4). The state variable is expressed by two equations, because it depends on the polarity of the input voltages, and it can be divided into two regions depending on the exiting state of the device, for more details [9]–[12].

$$f(x(t)) = \begin{Bmatrix} e^{-\alpha_p(x-x_p)}\omega_p(\mathrm{x},\mathrm{x}_p), \mathrm{x} \geq x_p \\ 1, \mathrm{x} < \mathrm{x}_p \end{Bmatrix} \quad (3)$$

$$f(x(t)) = \begin{Bmatrix} e^{-\alpha_n(x-x_n)}\omega_n(\mathrm{x},\mathrm{x}_n), \mathrm{x} \geq x_n \\ 1, \mathrm{x} < \mathrm{x}_n \end{Bmatrix} \quad (4)$$

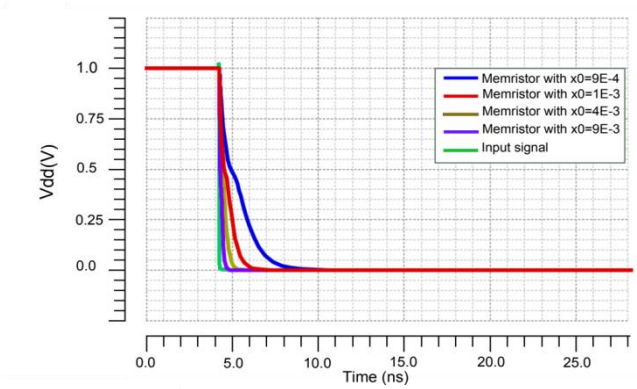
wherex_p; x_na boundary point, before these points the state variable is constant limited by an exponential function decaying by a rate either α_p,α_n.

III. USING MEMRISTOR AS A FILTER

The reliability metric is an important parameter in the integrated circuit industry, these circuits are designed to accomplish a certain task and it is expected to perform this job on each time of running, so if the circuit has completed its task as requested and planned it will be a reliable circuit. Soft errors are known as an obstacle to accomplishing this process because it makes the circuit works in unexpected mode (unreliable mode). It is possible to harden a circuit to partially prevent the effect of soft errors and increase the reliability of the circuit. In other words, pushing the running mode of the circuit to a more reliable region.

In this paper, we propose to use a memristor element as a filter to attenuate SET pulses that generated on combinational circuits. This proposal relied on previous studies, it has been found that neutron particles cause different glitches duration depending on their energies, so the narrow glitches that are generated on a circuit are affected by electrical masking and attenuated before they reach the output terminal. However, the glitches that are generated close to the output terminals can not be attenuated. So, it is not possible to rely on the attenuation effect to mitigate those glitches. On [13], it is suggested to use the last stage on a path as a filter by increasing its size to increase its inertial delay, so the narrow glitches can be attenuated. Memristor has been used as delay elements in some applications as in [8], [14], thus we propose to use a memristor (delay element) as a filter to be used to increase the reliability of digital circuits. Figure. 1 shows waveforms are passed through a memristor with different values of x_0, it can be noticed the delay time between the input signal and the output signals. Memristor size is measured by square nanometers, and it is compatible with CMOS components [15]–[19], these two reasons encourage us to use it with CMOS circuits.

Figure 1. Waveforms are registered at the input and the output terminals of a memristor connected to a digital circuit.



The model proposed by [20], has been chosen to be used in this paper as a delay element to filter glitches that are generated on prior stages, this model is used with Cadence simulation platform and connected between the last two stages to filter most of the generated glitches. Figure. 2 shows the connection of memristor on different paths of different circuits.

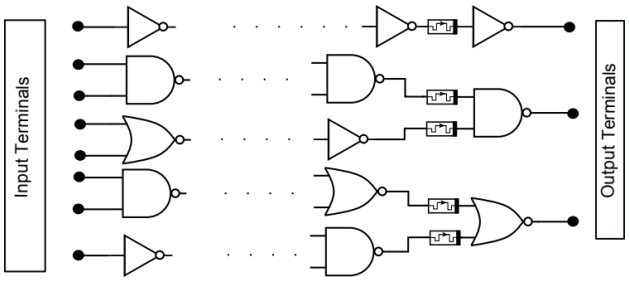


Figure 2. Memristor connected to different paths

IV. RELIABILITY IMPROVEMENT

In this section, the simulation results are introduced. These results are found by calculating the probability of soft errors using the proposed method on [21], after the probability of errors are calculated, the reliability of the circuit is derived by the relation $1 - (\text{probabilityoferrors})$.

The memristor filter is applied on three different circuits to see the effect of this stage on the reliability of those circuits, the candidate circuits were: a chain of inverters, ISCAS c432 benchmark, and ISCAS c1908 benchmark. In the next sections, more details will be found about these experiments.

A. A chain of inverters circuit

This circuit has been chosen to mimic single path circuits. This circuit consists of 205 inverters, all inverters are identical with specifications: pull-down NMOS transistor with length (L) = 80nm and width (W) =400 nm, pull-up PMOS transistor with L=80 nm and W=800 nm, a capacitor is placed between every two inverters to simulate the parasitic effect of the interconnection wires.

The memristor has connected between the last two inverters on the circuit, and different transient current pulses are injected on each inverter. The injected pulses cause glitches with different durations depending on the value of the LET. These glitches propagated through the path to be registered as a soft error at the output. The memristor works here as a filter stage with filtering efficiency depending on the memristance of the memristor. In each experiment, we changed the memristance of the memristor by changing the parameter x_0. The effect of the memristor on the reliability of the circuit is shown in Figure. 3, the experiment is conducted under different values of Vdd's to have a good understanding of how the voltage supply affects reliability.

The change of the reliability trend on different curves can be seen in Figure. 3, high reliable behaviour is obtained when the value of $x_0$is 9E-4 with this value, the memristance of the memristor was very high, this increase the propagation delay time witch causes attenuation of all the generated glitches. Only the glitches that are generated on the last stage (that stage after the memristor) are registered at the output of the circuit. Another value of $x_0$parameter has been chosen witch is 4E-3, and the reliability of the circuit calculated. It can be seen in the same figure the reliability of the circuit is not high as the previous value of x0 parameter, but still better than the reliability of the circuit without a memristor filter. The dashed lines on this figure show the 2D projection of the reliability curve with performance and energy consumption.

From Figure. 3 the reliability of the circuit can be tuned as required by changing the values of the x0 parameter, and also depends on the available resources (energy and performance).

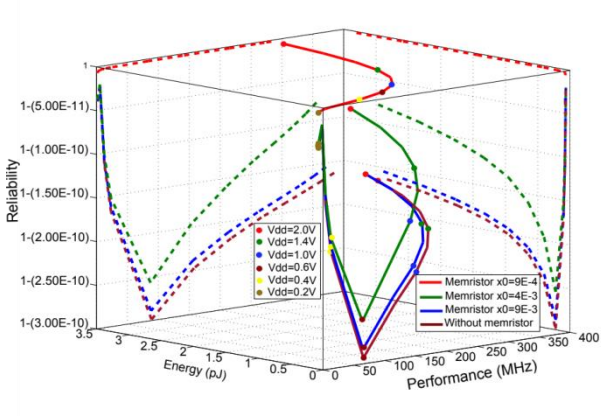


Figure 3. Energy-Reliability-Performance of chain of inverters circuit with and without the memristor filter

The suppression of the errors was the main reason to improve the reliability of the circuit. The strength of the suppression factor is proportional to the memristance increase. Figure. 4 shows the highest error suppression percentage occurred at $x_0$is 9E-4, where the minimum suppression percentage is occurred at $x_0$is 9E-3.

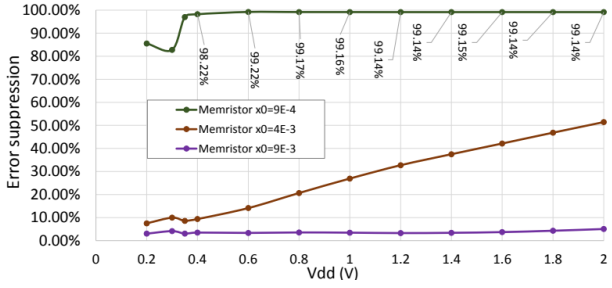


Figure 4. Error suppression percentages on the chain of inverters circuit vs V dd

B. c432 Benchmark

The proposed technique is applied on multipath circuit c432, this circuit is a channel interrupt controller that contains 36 input terminals, and 7 output lines. It is used here to see the effect of adding memristor filter stage on short path multipath circuits, the same procedure is adopted as on the last section, so the reliability of the circuit is derived without memristor stage, and then the experiment is repeated with memristor for different values of parameter x_0, the results are similar to the previous one (chain of inverters case), with minor differences related to the circuit topology, but the trend of reliability curve is almost same in the two cases. It can be seen from Figure.5 the circuit works in a high reliable state when $x_0$is 9E-4, and the reliability does not depend on the Vdd as in the other cases of x0 or in the case of the

circuit without memristor. This is because the memristor stage filtered all the glitches that generated in the prior stages.

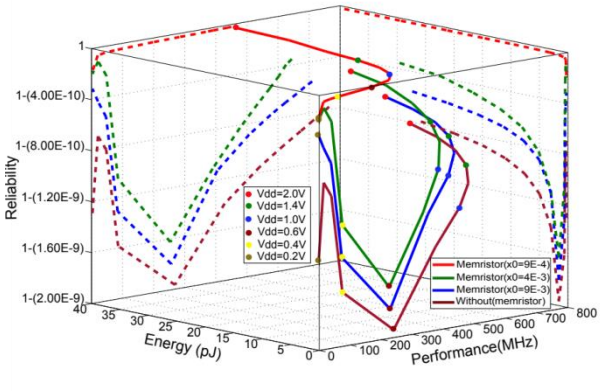


Figure 5. Energy-Reliability-Performance of c432 circuit with and without the memristor filter

The error suppression percentages are illustrated in Figure.6, it is clear that the error suppression is more than 95% when the memristor with $x_0$is equal to 9E-4 is used. In the other two cases with $x_0$is equal to 4E-3 and 9E-3 this percentage is lower, and the error suppression depends on the Vdd. Therefore, it can be seen in the same figure at high Vdd values where the error probability is not high the suppression percentage is high, and this percentage decreases gradually until Vdd = 0.4 V the suppression percentage starts increasing and reliability also increases.

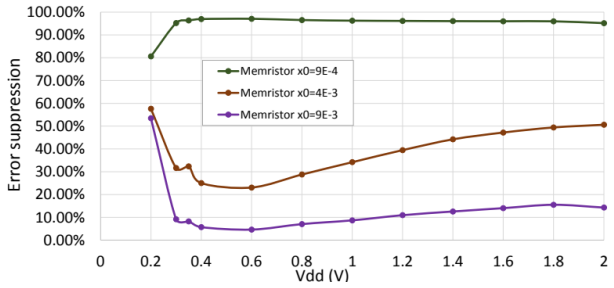


Figure 6. Error suppression percentages of c432 circuit vs V dd

C. *c1908 Benchmark*

The proposed technique is applied on the ISCAS c1908 benchmark, this circuit works as a 16-bit error detector/corrector, with 33 input and 25 output terminals. This circuit is chosen to explore the effect of memristor element on the soft error probability on long path multipath circuits, the same procedure is applied in this case, so the probability of soft errors is calculated before and after adding the memristor stage to the circuit, the memristor element is applied to the circuit with thee different values of the initial state variable x_0.

Figure.7, shows the trade-off relation between Energy, Performance, and Reliability. It can be seen from the figure the highest reliable performance is obtained when the parameter $x_0$is 9E-4, the reliability curve is very close to the value 1, which means high reliable execution at this level. The dotted lines in the figure represent the projection of the reliability curves on the 2D graph of reliability curve, so one surface represents changing the reliability with performance and the other one represents changing the reliability with energy, from which it is possible to obtain the full notion on the reliability trend.

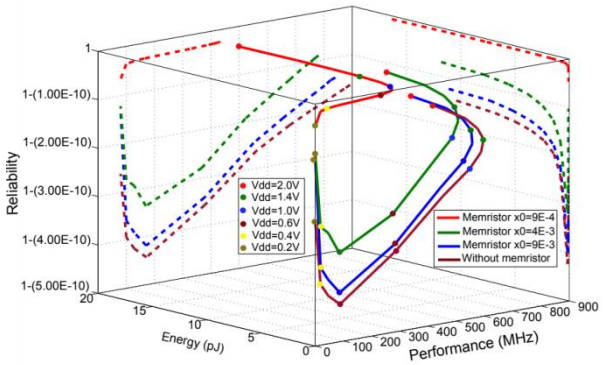


Figure 7. Energy-Reliability-Performance of c1908 circuit with and without the memristor filter

To have a good understanding of the effect of adding memristor element on the error probability, Figure.8 shows the percentage of error reduction that obtained at different values of x_0, and different values of Vdd. At $x_0$is equal to 9E-4, the error suppression is not related to the Vdd, but at the other two values, it changes depending on Vdd values to be at the highest levels at subthreshold voltages.

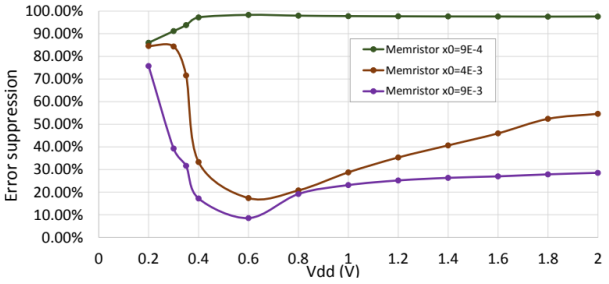


Figure 8. Error suppression percentages of c1908 circuit vs V dd

By comparing the reliability improvement that is achieved by adding the memristor stage with the reliability of the circuit without this stage, we will find that the performance or the energy consumption that is needed to achieve the same reliability level without adding the memristor stage is higher than the energy consumption or the performance that is needed to achieve with the memristor stage.

V. THE EFFECT OF THE PROPOSED TECHNIQUE ON CIRCUIT PARAMETERS

As is mentioned in the aforementioned sections, there is a trade-off relation between the three parameters; Energy, Performance, and Reliability. By adding the memristor stage the circuit gained more reliability, and this gain is clear on the previous figures Figure.3, 5, 7, by moving the trend of the reliability curve upward to a higher level and closer to 1. This improvement in reliability is obtained by effecting a reduction in the circuit performance and increasing energy consumption.

In this section, the performance reduction and the energy consumption increase percentages are introduced. However, if we compare the same performance of the original circuit (the circuit without the memristor element) and the circuit after adding the memristor element, we will find that the reliability is improved by adding the memristor stage. This is applicable to energy consumption too.

The effect of the memristor stage on the performance of the chain of inverters circuit is shown in Figure.9, it can be seen that the performance is affected most with the memristor stage with $x_0$equal to 9E-4, where at this value of initial state variable the reliability improvement level was the highest.

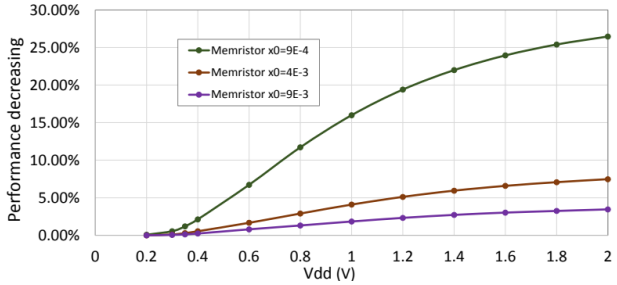


Figure 9. The effect of memristor stage on the Performance of the chain of inverters circuit

Figure.10 shows the effect of the memristor stage on the energy consumption, the higher energy consumption has occurred when the memristor with$x_0$is equal to 9E-4 is connected to the circuit, the energy consumption is proportional with Vdd.

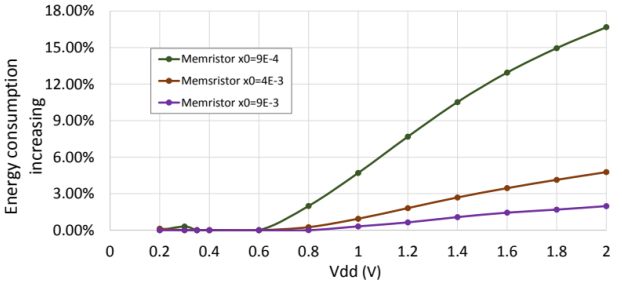
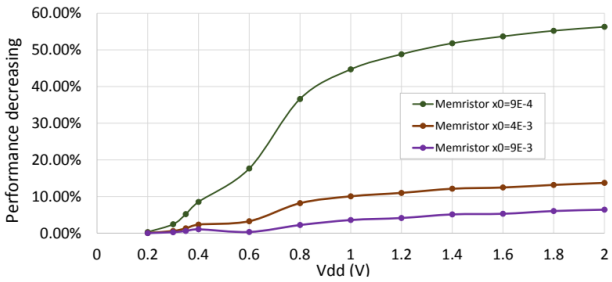


Figure 10. The effect of memristor stage on the energy consumption of the chain of inverters circuit

The reduction in the performance of the c432 circuit is studied at the three chosen values of x_0, as we mentioned earlier this circuit is chosen to represent short paths circuit, so in this type of topology, each stage relatively has a large contribution on the performance of the whole circuit, Figure.11 shows that the highest reduction percentage has occurred with $x_0$equal to 9E-4, and if we compared between Figure.9 and Figire.11 it can be noticed that c432 circuit is affected by the reduction in the performance more than the chain of inverters circuit, that is because the logic depth of c432 circuit is less than the logic depth of the chain of inverters circuit.

Figure 11. The effect of memristor stage on the c432 circuit's performance

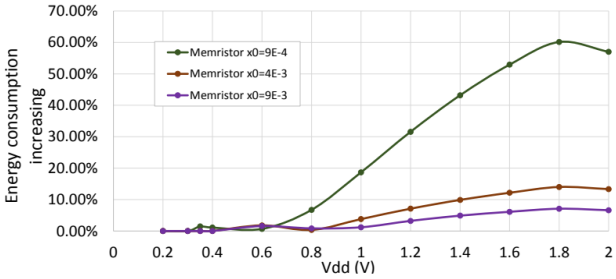
The energy consumption increased by adding the



memristor stage, the percentage of this increase is illustrated in Figure.12, the maximum increase is 60%, which occurred at Vdd = 1.8V, and at Vdd lower than this value the increasing percentage is decreased to a negligible value at Vdd lower than or equal 0.6V.

Figure 12. The effect of memristor stage on the energy consumption of c432 circuit

The last circuit is used to examine our technique is the c1908 circuit, as we mentioned earlier this circuit is



considered as a long path circuit, the effect of the memristor stage on performance and energy consumption will be less, compared with the c432 circuit. Figure.13 shows the effect of the memristor stage on the performance of c1908, the maximum reduction percentage is around 45%, which occurred at Vdd = 1.6V. In the other two cases when the x_0 is equal to 4E-3, and 9E-3, where the maximum reduction on the performance was 15% and 7% respectively, these values can be considered small values compared to the improvement that occurred on the reliability.

Figure.14, introduces the effect of the memristor stage on the energy consumption of the c1908 circuit, it can be seen that the maximum increasing percentage is 52%, this value has occurred at Vdd = 2V, but this percentage is decreased at lower Vdd values, For example, at Vdd = 1 V, this percentage is 16% where the reliability is improved at the highest level at this Vdd value.

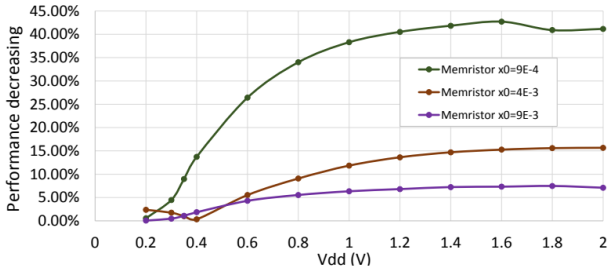


Figure 13. The effect of memristor stage on the c1908 circuit's performance

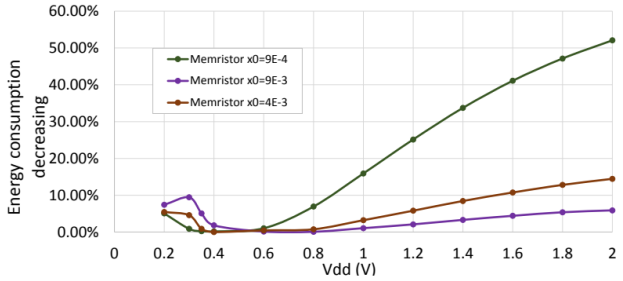


Figure 14. The effect of memristor stage on the energy consumption ofc1908 circuit

By looking at these figures and the reliability figures, the provider can choose the best x_0 parameter value that achieves a good reliability level, depending on the criticality of the required task.

VI. CONCLUSIONS

The main achievement reported in this paper is using a memristor element to improve the reliability of digital circuits. In this paper, the memristor element is used as a filter stage to increase the resilience of the circuit and make it less sensitive to soft errors.

The reliability metric of digital circuits is improved by adding this stage. The memristor is examined by changing the value of x_0 parameter between three values to show its effect on the reliability improvement. The best reliability level is achieved at x_0 is equal to 9E-4. The effect of this stage on the performance and energy consumption is studied to build a complete understanding of the advantages and disadvantages of this element. The area overhead is not a big concern as this element is already fabricated at a nanoscale level, so it has not been taken on our simulation account.

REFERENCES

[1] V. Ferlet-Cavrois, L. W. Massengill, and P. Gouker, "*Single event transients in digital cmos*," IEEE Transactions on Nuclear Science, vol. 6, no. 1, pp. 1767–1790, 2013.

[2] G. B. Hamad, S. R. Hasan, O. A. Mohamed, and Y. Savaria, "*New insights into the single event transient propagation through static and tspc logic*," IEEE Transactions on Nuclear Science, vol. 61, no. 4, pp. 1618–1627, Aug 2014.

[3] M. Ebrahimi, A. Evans, M. B. Tahoori, E. Costenaro, D. Alexandrescu, V. Chandra, and R. Seyyedi, "*Comprehensive analysis of sequential and combinational soft errors in an embedded processor*," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 34, no. 10, pp. 1586–1599, Oct 2015.

[4] M. Raji, B. Ghavami, and H. Pedram, "*Gate resizing for soft error rate reduction in nano-scale digital circuits considering process variations*," in 2015 Euromicro Conference on Digital System Design, Aug 2015, pp. 445–452.

[5] F.-X. Yu, L. Jia-Rui, H. Zheng-Liang, L. Hao, and L. Zhe-Ming, "*Overview of radiation hardening techniques for ic design*," vol. 9, 06 2010.

[6] L. Chua, "*Memristor-the missing circuit element*," IEEE Transactions on Circuit Theory, vol. 18, no. 5, pp. 507–519, September 1971.

[7] R. S. Williams, "*How we found the missing memristor*," IEEE Spectrum, vol. 45, no. 12, pp. 28–35, Dec 2008.

[8] S. M. A. B. Mokhtar and W. F. H. Abdullah, "*Memristor to control delay of delay element*," in 2014 IEEE International Conference on Semiconductor Electronics (ICSE2014), Aug 2014, pp. 483–486.

[9] Z. Biolek, D. Biolek, and V. Biolkov´a, "*Spice model of memristor withnonlinear dopant drift*," Radioengineering, pp. 210–214.

[10] Y. N. Joglekar and S. J. Wolf, "*The elusive memristor: properties of basic electrical circuits*," European Journal of Physics, vol. 30, no. 4, p. 661, 2009.

[11] C. Yakopcic, T. M. Taha, G. Subramanyam, and R. E. Pino, "*Generalized memristive device spice model and its application in circuit design*," IEEE Transactions on Computer-Aided Design of Integrated Circuitsand Systems, vol. 32, no. 8, pp. 1201–1214, Aug 2013.

[12] M. Laiho, E. Lehtonen, A. Russell, and P. Dudek, "*Memristive synapses are becoming reality*," 2010.

[13] M. A. Abufalgha and A. Bystrov, "*Derivation of the reliability metric for digital circuits*," in 2017 22nd IEEE European Test Symposium (ETS), May 2017, pp. 1–2.

[14] X. Zhang, Z. Ma, J. Yu, and L. Xie, "*Memristor-based programmable delay element*," in 2014 12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Oct 2014, pp. 1–3.

[15] Q. Xia, W. Robinett, M. W. Cumbie, N. Banerjee, T. J. Cardinali, J. J. Yang, W. Wu, X. Li, W. M. Tong, D. B. Strukov, G. S. Snider, G. Medeiros-Ribeiro, and R. S. Williams, "*Memristor cmos hybrid integrated circuits for reconfigurable logic*," Nano Letters, vol. 9, no. 10, pp. 3640–3645, 2009, pMID: 19722537.

[16] K. Cho, S.-J. Lee, and K. Eshraghian, "*Memristor-cmos logic and digital computational components*," Microelectronics Journal, vol. 46, no. 3, pp. 214 – 220, 2015.

[17] Y. Guo, X. Wang, and Z. Zeng, "*A compact memristor-cmos hybrid look-up-table design and potential application in FPGA*," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 36, no. 12, pp. 2144–2148, Dec 2017.

[18] M. Teimoory, A. Amirsoleimani, A. Ahmadi, and M. Ahmadi, "*A hybrid memristor-cmos multiplier design based on memristive universal logic gates*," in 2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS), Aug 2017, pp. 1422–1425.

[19] D. B. Strukov, D. R. Stewart, J. Borghetti, X. Li, M. Pickett, G. M. Ribeiro, W. Robinett, G. Snider, J. P. Strachan, W.Wu, Q. Xia, J. J. Yang, and R. S. Williams, "*Hybrid cmos memristor circuits*," in Proceedings of 2010 IEEE International Symposium on Circuits and Systems, May2010, pp. 1967–1970.

[20] R. Naous, M. Al-Shedivat, and K. N. Salama, "*Stochasticity modeling in memristors*," IEEE Transactions on Nanotechnology, vol. 15, no. 1, pp. 15–28, Jan 2016.

[21] M. A. Abufalgha and A. Bystrov, "*Design-time reliability evaluation for digital circuits,"* in 2017 IEEE 23rd International Symposium on On-Line Testing and Robust System Design (IOLTS), July 2017, pp. 39–44.

[22] Y. Ibrahim *et al*., "*Soft Error Resilience of Deep Residual Networks for Object Recognition*," in *IEEE Access*, vol. 8, pp. 19490-19503, 2020, doi: 10.1109/ACCESS.2020.2968129.

[23] J. Prinzie and V. De Smedt, "*Time-Dependent Single-Event Effects in CMOS LC -Oscillators*," in *IEEE Transactions on Nuclear Science*, vol. 66, no. 9, pp. 2048-2054, Sept. 2019, doi: 10.1109/TNS.2019.2930414.

BIOGRAPHIES

Mohamed A. Abufalgha received the B.S. and M.S. degrees in electronic and computer engineering from Almergib University, Alkhoms, Libya in 1997 and 2007 and the Ph.D degree in electronic engineering from Newcastle University, Newcastle, United Kingdom in 2019. He is currently a lecturer of electrical and computer engineering with Misurata University, Misurata, Libya, where he teaches microelectronic circuits analysis and design and studies the effects of radiation on the reliability of integrated circuits. His research interests include soft errors and the relation between reliability of digital circuits and the energy consumption with emphasis on design techniques to characterize and mitigate soft errors.